BEST: International Journal of Management, Information Technology and Engineering (BEST: IJMITE)
ISSN (P): 2348-0513, ISSN (E): 2454-471X
Vol. 4, Issue 9, Sep 2016, 43-66

PERSPECTIVE ON CONSCIOUSNESS -- SPECIALIZED NEURONS, THEIR CHARACTERISTICS AND THEIR CIRCUITRY

JOHN ROBERT BURGER

PhD, California State University Northridge, California

ABSTRACT

This article introduces a fresh theory of consciousness based on complex neural circuitry, as envisioned from the novel perspective of electrical circuit science. Circuit science goes well beyond molecular science to show a need for certain specialized neurons during everyday brain operations. For example, it is found that certain neurons must support single pulses where accurate timing is required, as essential to an efficient mental system. In related instances, precise control is mandatory, requiring neurons that can be made self-active for a time, but that are easily toggled between active and rest. The article below describes such neurons, and other essential neurons theoretically necessary to generate a plausible mental structure capable of consciousness.

KEYWORDS: Complex Neural Circuitry, Neurons

INTRODUCTION

Sooner or later everyone thinks about, or is curious about the physical underpinnings of consciousness. Over one hundred billion little cells or neurons are interconnected in a certain way to provide what we experience subjectively as consciousness. Related to consciousness would be rudimentary thinking, given that one thought often follows another, a topic of some interest. What is missing, and difficult to find is how exactly those billions of little neurons are connected? Likewise missing is a satisfying physical explanation of consciousness.

Many are baffled by the complexity of neural interconnections. Indeed, special training is required for analyzing and understanding complex interconnections. Scientists tend to be exceedingly knowledgeable about ions and molecules, as clearly evidenced by textbooks on neuroscience. But unfortunately, ions alone can never explain something as complex as an interconnection of neurons in a brain.

The work reported below concerns neurons as specialized components operating in a complex interconnected environment. Neurons work together only under certain exacting conditions, and uncovering these conditions can be extremely important to all concerned.

SCOPE OF THIS ARTICLE

The field of Neural Circuits and Neural Systems (NCAS) strives to explain consciousness physically, using circuit theory as applied to neurons. NCAS generally focuses mainly on the behavior of a complex interconnection of neurons, and so differs fundamentally from the ever popular approaches using molecular biology and biochemistry.

Instead of ion transfers, neural circuitry is characterized by thousands of signals working in parallel; NCAS is concerned about where they begin, what they do, and where they end. Inescapably linked to this are various systems of memory based on neurons.

The translation of sensory information or perceptions into attributes is nontrivial and important, but is beyond the scope of this article. Sensory information, such as sights, sounds, smells, touches and so on, are assumed to have been decoded into fundamental attributes, each signaled by individual nerve pulses. Attributes, incidentally, are such parameters as brightness, color, size, shape, tone, intensity and a finite host of elementary descriptors as derived from the senses.

NCAS is not about artificial neurons; nor is it about artificial neural networks, or any other system of computerized simulation. Computerized simulation, even using the most powerful of computers, falls far short of accomplishing what most humans achieve effortlessly: Common sense, truth judgment, intuition, artistic appraisal and other hallmarks of humans. NCAS, in contrast, aims not to simulate, nor to engineer, but to understand systems of neurons, with thoughtful analysis and synthesis to determine how they work together**.**

DEFINITION OF CONSCIOUSNESS

Consciousness is defined here to be the quality of being aware of external objects, including feelings within oneself that these external objects bring forth from long-term memory. This definition necessitates an ability to recall memories associated with perceptions delivered from the senses. Consciousness, under this definition, depends on a significant store of information, indeed all past relevant events.

Simple household systems, such as a thermostat are not conscious under this definition, since they have almost no memory. Computers as we know them also do not generally maintain records of all past experiences; and so under this definition, they also are not conscious. Of course, a sophisticated robot can be responsive to its environment, but generally they currently are unable to recall related ***experiences, to predict foreseeable events, to "feel" and to connect to a given scene.***

Associative Memory in Humans

It is useful to think of sensory information as being imposed on short-term memory. The contents of short-term memory can be assumed to alternate between images from the senses, and associative recalls from long-term memory. In this way a person is quickly aware of physical danger, for example, based on what he or she sees, hears, or otherwise perceives, and thus is able to recall protective responses as remembered from past experiences.

A major relationship between what is perceived and what is remembered is association, possibly association with a very minor component of a current image. An image always has components, although components need not be what the image is about. Note that an "image" in this context is not just a simple picture, but is a recollection of sights, sounds, smells, feelings etc. as pulled from long-term memory.

The cues for association can range from a small part of the content of an image to nearly all of the content of an image. Nearly all of the content is used when turning the same image or thought over and over in one's head, considering differing angles. Turning-over a given thought can convert an incomplete image into a better image.

Producing memories using only a small component of an image is a form of brain-storming, in which a vague unnoticed detail in a mental image is permitted to produce unexpected returns from subconscious long-term memory.

Turning-over a given thought as well as brain-storming are widely accepted ***forms of association that most everyone has experienced.***

Short-Term Memory Using Neurons

To support a mental operation, short-term memory neurons are most helpful, since they hold attributes derived from sensory inputs, and they also hold recalls from long-term memory. Short-term memory neurons hold their information long enough to facilitate a search of long-term memory during a recall process. To better explain short-term memory neurons, the salient parts of one may be diagrammed as in Figure 1 (note all neurons differ; this is only an instructive diagram).

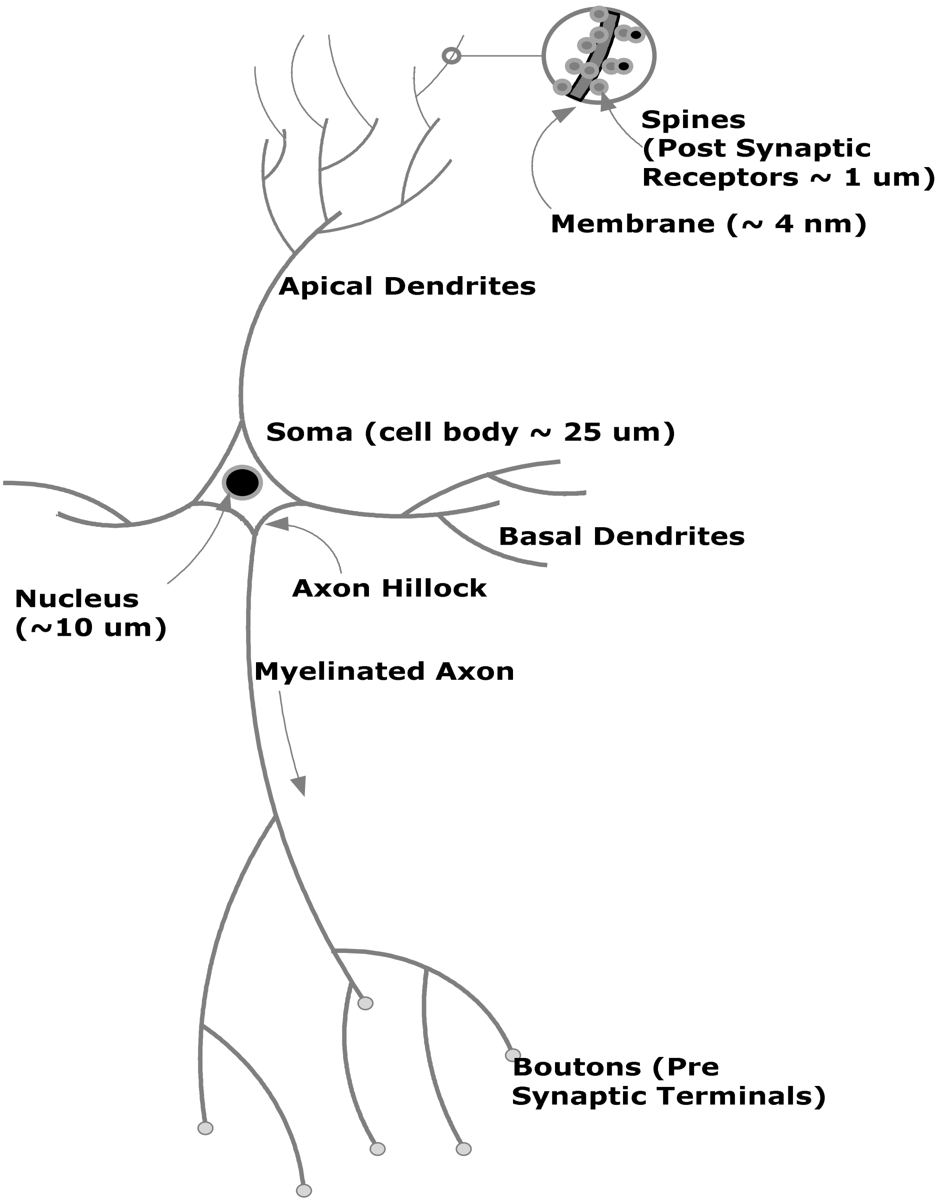

Figure 1: Parts of a Neuron

Any neuron is naturally a short-term memory neuron, since a neural pulse burst records the existence of a signal for a few milliseconds (Figure 2).

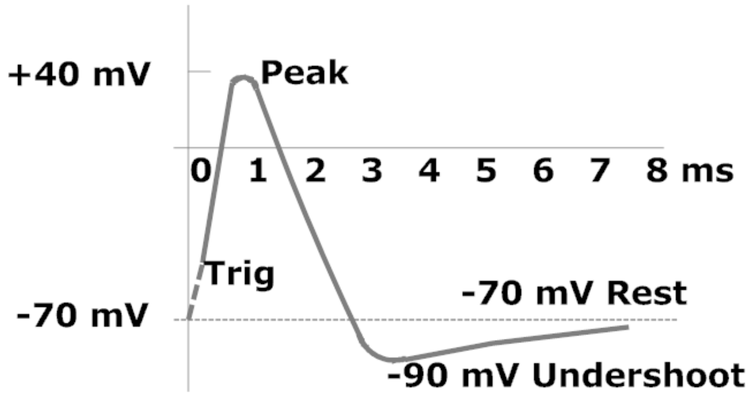

Figure 2: Typical Neural Pulse Waveform, Inside Relative to Outside

A pulse in a dendrite with an especially long duration, or pulse width, could be achieved by interfering with the charge transfers that cause a neural pulse across a membrane to recover to rest, or to recover to a potential of about -70 mV in the above waveform. If there is a significant shortfall in the density of internal potassium ions within a neuron, for example, this would reduce the capture of negative charge from outside the neuron, thus producing a much longer pulse in the dendrite.

When such a long pulse reaches the soma (or body) of the neuron, the soma is "super-triggered," resulting in a long burst of pulses traveling to connecting neurons. The resulting pulse train is assumed to last for up to several seconds (Figure 3). This pulse ***burst clearly signals the presence of a given attribute.***

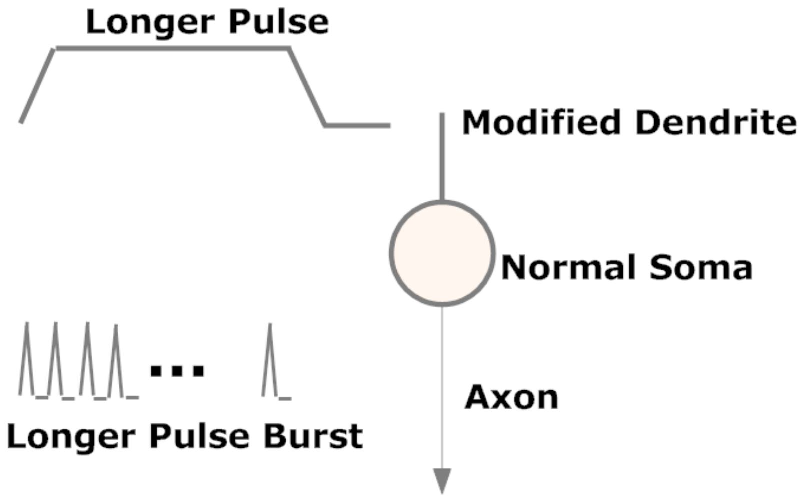

Figure 3: Diagram of a Short-Term Memory Neuron

Short-term memory is assumed to serve up to ***K*** attributes (***K*** is not specified here). These attributes connect to corresponding elements of long-term memory during a memory search. Such searches occur in response to new perceptions by the senses, but they could also occur in response to recent recalls from long-term memory. Short-term memory is envisioned to be connected as suggested in Figure 4.

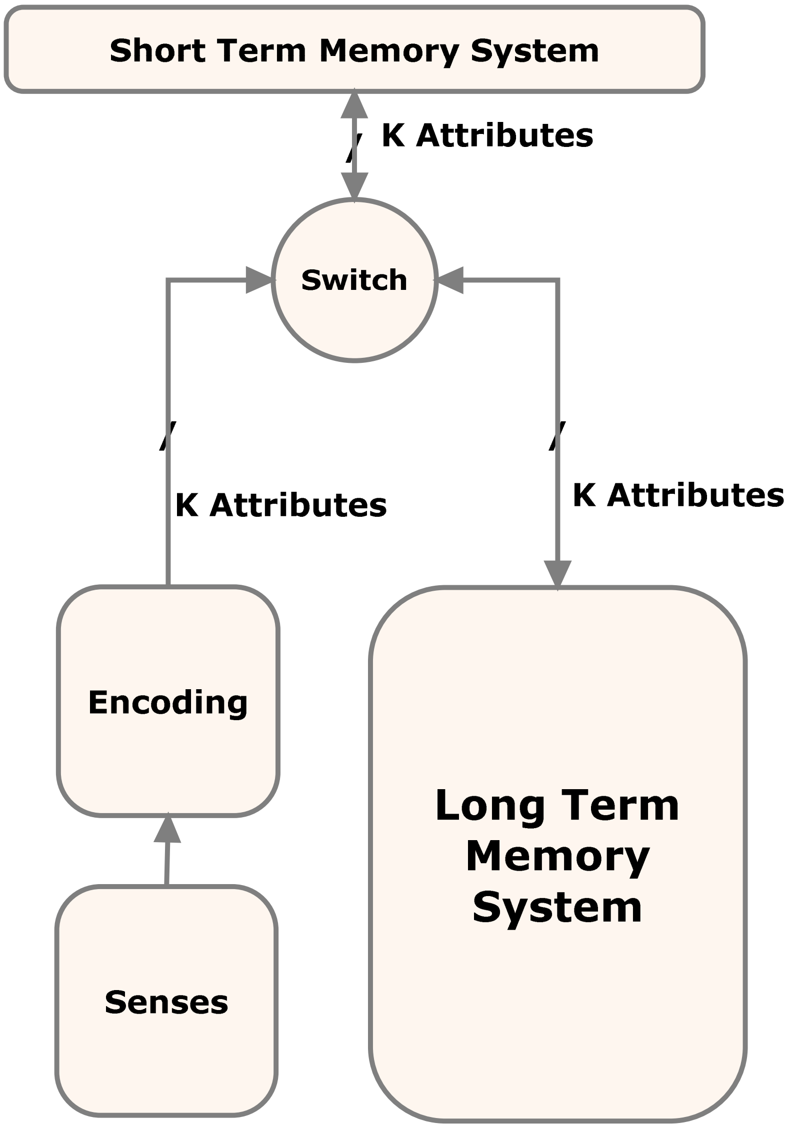

Figure 4: Alternating Perceptions and Recalls

Switching between perceptions and recalls is easily accomplished with ordinary neurons (Basic neural logic is introduced in **Attachment 1**). Switching between perceptions and recalls occurs fairly rapidly. A person sees an image; then the person experiences a recall derived from that image, a recall that may suggest a course of action. Note that new images are assumed impressed over past images such that the most recent predominate.

Long-Term Memory System

A long-term memory system can be visualized as a system as illustrated in Figure 5. Although neurons are tremendously plentiful, it is important to note that a given image uses only a small fraction of the available attributes, so in this sense, distributed long-term memory is sparse. Subconscious long-term memory may be assumed to correspond logically, attribute for attribute, with short-term memory, since images routinely pass between the two. Of course, memory neurons are not lined up in any particular way physically. But they are connected logically; a dedicated short-term memory neuron exists for each important feature, and there is a path to a corresponding element within long-term memory.

The little dots in the figure represent possible long-term memory elements, most of which are not used. Given a sparse distributed memory, many images, ***L*** in number (***L*** is not specified here) are possible using a modest number of neurons. The *Biological Editors* in the figure help ensure that each memory search eventually finds something, and that what is presented to consciousness is of maximum importance.

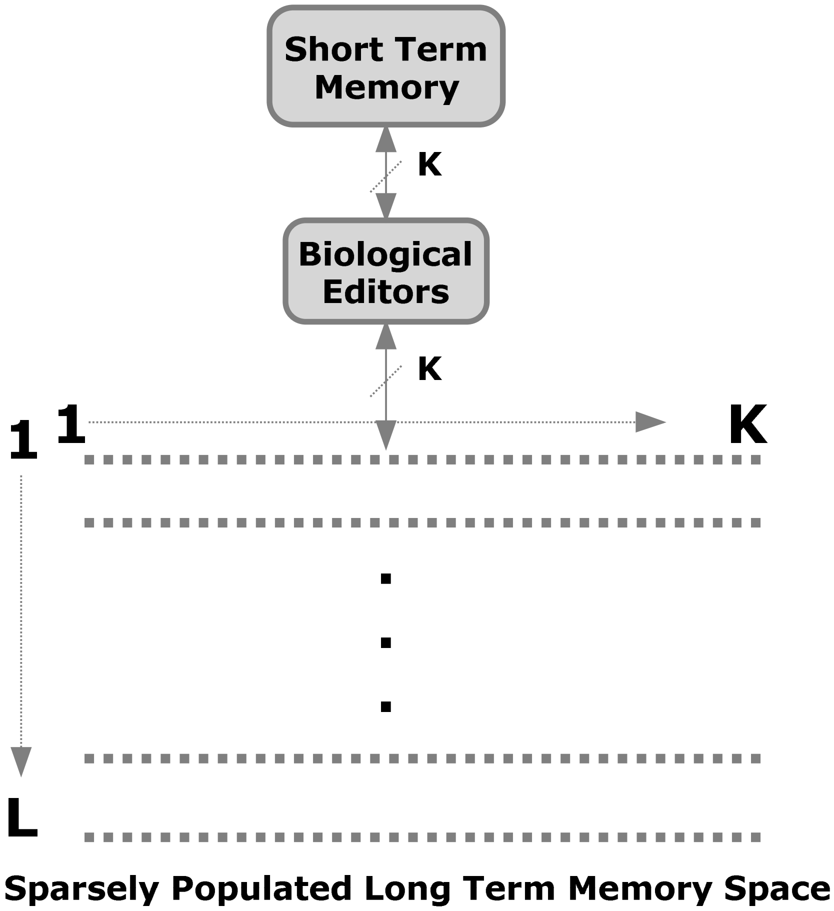

Figure 5: Short-Term and Sparse Long-Term Memory

Long-Term Memory Neurons

There are various ideas about how neurons realize long-term memory. One of the simplest assumes ability for long-term potentiating (LTP). LTP may be described as a pre charge that is held by a special receptor, making it easier for that receptor to be triggered.

To understand how LTP is utilized, we first note that it is helpful to define a "*weak*" synapse. Usually, when a synapse is activated, several pulses are emitted in the form of a burst. There may be ten pulses in a group, thought to be due to charged neurotransmitters oscillating within the cleft of the synapse. But when a weak synapse is activated, it produces only a single pulse in its dendrite. This could be done with neural logic, but it is easier to produce a single pulse using the geometry of a synapse. The open geometry in Figure 6 would prevent the expected lingering of neurotransmitters within the synaptic cleft, a possible source of several pulses within a burst.

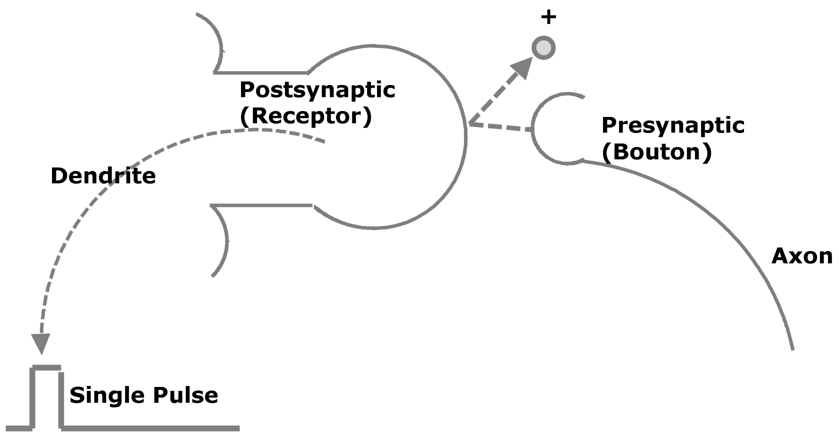

Figure 6: Weak Synapse Emitting a Single Pulse

Long-term potentiating is assumed instilled by a burst of pulses to a LTP synapse, which causes charge (labeled LTP) as in Figure 7, to be held in a special receptor in a long-term memory neuron. Subsequently the neuron is queried with a READ signal, resulting in a single read pulse ***R*** from a weak synapse. Without LTP a single pulse would not induce enough charge to trigger a neural pulse, giving no output at ***Q***. The memory element produces output if and only if LTP is present; output at ***Q*** denotes an active attribute. This form of memory would require two neurons, one for an input OR gate, and one with LTP capability as an output neuron.

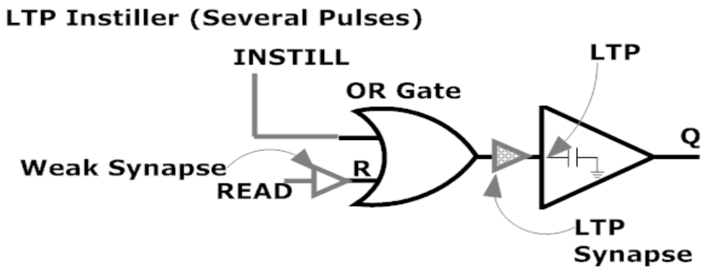

Figure 7: Long-Term Memory Sub Circuit

The neural OR, by the way, is merely a dendrite with two branches connected to a trunk (Refer to **Attachment 1**).

System for Long-term memory

A subset of the active (or true) attributes in short-term memory is readily available to serve as cues for an associative search of long-term associative memory. As typical of associative memory, if there are only a few cues, there will be many matches, if there are many cues, there will be very few matches. A search begins with a memory enable signal, labeled ***E*** in Figure 8; after this, the entire system of long-term memory is queried essentially in parallel, to find matches to the applied cues.

It is easier (using neural logic) to find matches using only to those cues that are active, or true. A simplified system is described in **Attachment 2.** What is returned will exactly match the cues that are active (true). This approach is likely to return a useful image, especially when there are many true cues.

When cues tend to be few, more than one match is expected, necessitating a method of *multi-match resolution*. As in any associate memory system, the first step is to categorize matches one at a time. Neural logic can do this without difficulty, as long as the possibility of a toggle neuron is included (toggle neurons are discussed in **Attachment 3**). An element of an image, or word of associative long-term memory (one of a great many) can be envisioned as in Figure 8.

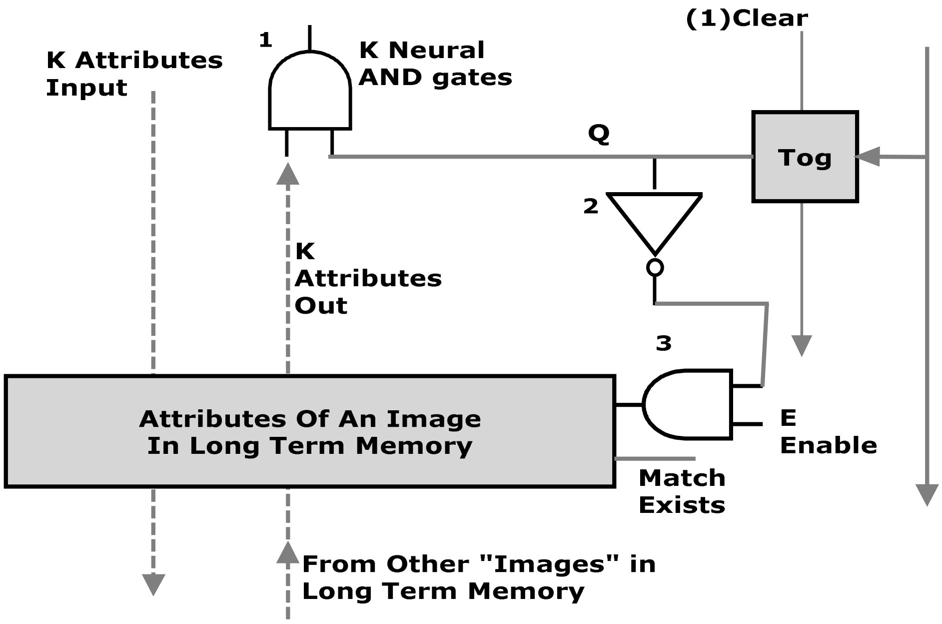

Figure 8: System for Reading a Long-Term Memory Image

To begin, up to K cues (at the "K Attributes Input") flow (down). Long-term memory elements, once enabled, are such that matches, if they exist, are identified by an output signal from the stored image. This "match exists" signal is held temporarily within the word as long as E is applied.

Toggle neurons conveniently serve to sequence the matches (refer to the block labeled Tog in the figure). Initially all toggles are cleared. Because of the "K neural AND gates" labeled 1, the outputs from any given word cannot transmit to words above. Next, a traveling single pulse then propagates asynchronously, and triggers to true the first toggle it encounters. If there is a match, this enables that particular match to be returned (via gates 1). The active toggle disconnects the enable signal E from that word (via gate 3 in the figure), so this image cannot be returned more than once.. The neural logic is such that once the enable E is removed, a word of long-term memory become transparent, meaning it passes signals from below.

The traveling pulse subsequently sets to true the toggle attached to the next matched word, and similarly facilitates the return of successive matched images. Matched images from long-term memory are delivered one at a time, asynchronously, each with up to K attributes. They flow "up" on their dedicated axons, parallel to the paths by which the search cues were initially delivered. These returns are going to be captured by a "return editor" described below, so that only the most important is permitted into short-term memory, to replace the current image from which cues were taken.

Memory Failures

Sometimes there is a failure to remember, known as a memory block. In physical terms, this means that the cues are inconsistent. As a result, no returns occur after a memory search. It is known, however, that later, perhaps hours later, the sought after memory sometimes pops into consciousness. This can be explained as a process in which the inconsistent cues are stored and modified by randomly removing one or more cues, and performing another search. If still no return, cues are reinstated, and different cues are removed for another try, all subliminally.

Cue editing might work as follows. When a mental block occurs, active cues may be diverted to a register of toggle neurons; the attributes are held in toggles connected to produce maximal frequency f2, essentially square waves. A simple method (see Figure 9) permits the removal of a small number of active cues randomly.

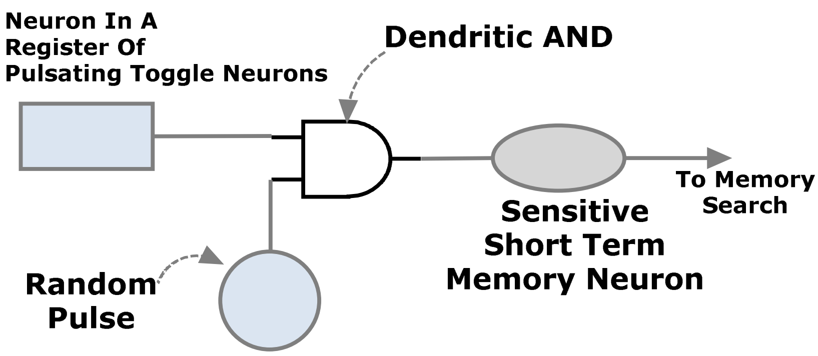

Figure 9: Removal of a Small Number of Active Cues

The random pulse is assumed generated by a special receptor that is sensitive to an energetic ion impinging on the receptor, as expected randomly in a thermal distribution. The neural AND gate has the power to remove an attribute during a memory search. Normally no attributes are removed as suggested by Figure 10 (top); a sampling pulse always passes the given attribute at f_2 no matter when the random pulse occurs.

But if the toggles are made to produce a lower frequency f_1, perhaps using a neurotransmitter-induced change, equivalent to increased delay in the loop, the situation changes. The chance is lower that a sample pulse will overlap an attribute pulse sufficiently to pass enough charge to trigger the short-term memory neuron (Figure 10 bottom). Consequently a given attribute can be made to appear inactive for the purposes of a memory search.

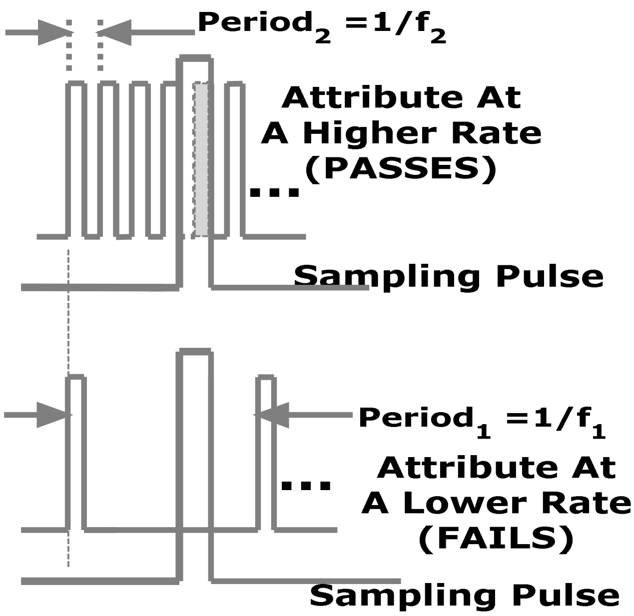

Figure 10: Effect of Attribute Rate in a Sampled System

Editing of Returns from Long-Term Memory

The subconscious editing of returns from long-term memory can be related to something that gifted savants often display fast mental arithmetic. Savants, known as “mental calculators” excel at rapid multiplications, divisions, roots, powers and prime numbers recognition and other calculating skills. Efficient mental processing is one of the best explanations of their skills.

Many calculating tasks can be visualized as massively parallel sets of operations followed by simple accumulation. For example, when multiplying two large numbers, the multiplicand may be multiplied by each digit of the multiplier in parallel. Then the partial products can be added to determine the product. Multiplying 678 by 345, for example, can be accomplished by multiplying 678 by 3, while concurrently multiplying 678 by 4, while concurrently multiplying 678 by 5; the product is simply a weighted sum of the partial products.

Toggle Neurons for Fast Arithmetic

It has long been known that controlled toggles are capable of massively parallel computing. Controlled toggles are those that toggle only if a control signal is true. One can envision a structure as in Figure 11.

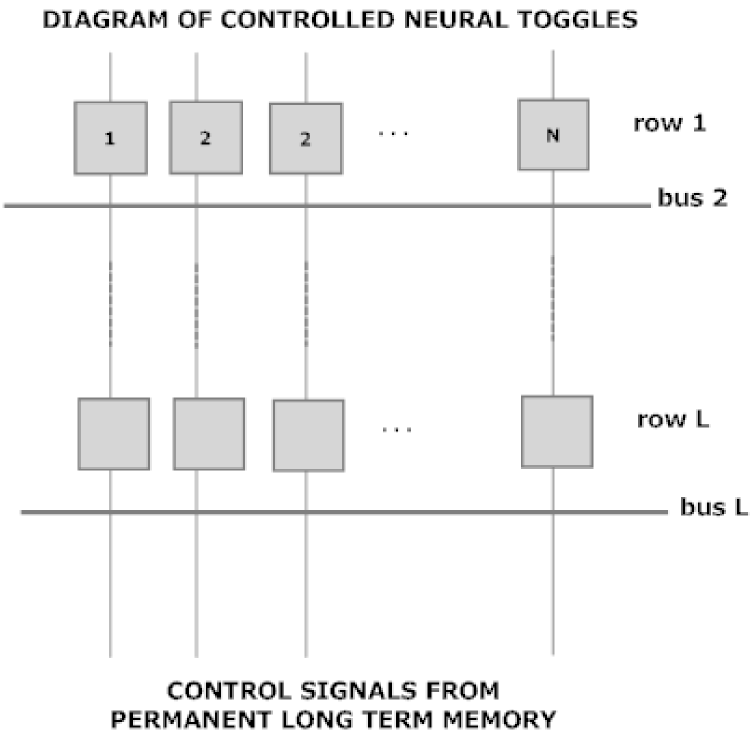

Figure 11: Plan for controlled-toggle computing

Controlled toggle neurons are organized into rows, or registers, where register size N exceeds the maximum number of attributes in an image, or components in a large number. Each register has extra toggle elements, serving as "scratchpad" space for computing. The number of registers or rows is assumed to be L, which might correspond to L different images.

Computations are carried out using steps in which the contents of individual toggles in a register are used to decide if some other toggle in that register needs a change of state (toggling). The steps are controlled by signals previously stored in long-term memory, and for efficiency, can be brought forth asynchronously (coming from "below" in the figure). These steps are executed in parallel within each register. Details are standard fare (and well known) in the field of reversible (massively parallel) computing (examples are not delineated here). A final accumulation, if needed, can be accomplished with ancillary neural logic, to efficiently obtain a result.

Memory Return Editing

Return editing might be done might be done as follows. Return editing can be envisioned as the adding together of weights associated with certain image attributes, those that define what is important (for survival). Available are measures of physical danger, emotional intensities, loudness, brightness of perceptions, number of cues, and perhaps a few other factors. Each return from long-term memory will have these critical attributes available within the returned image in a fixed location. These critical attributes are next weighted with a binary factor of say, N1 bits, to measure importance, where N1 is a small integer. Binary codes are convenient for humans, but other codes are possible. Adding these binary codes in parallel for each image or word will establish a priority value for that image.

An ancillary network of neurons can serve to select that image priority with the highest magnitude, and subsequently switch that image into short-term memory, or consciousness. For readers with a procedural turn of mind, Figure 12 suggests a plan that would efficiently and asynchronously choose the highest priority return from among those returns brought up from long-term memory, and direct it to consciousness.

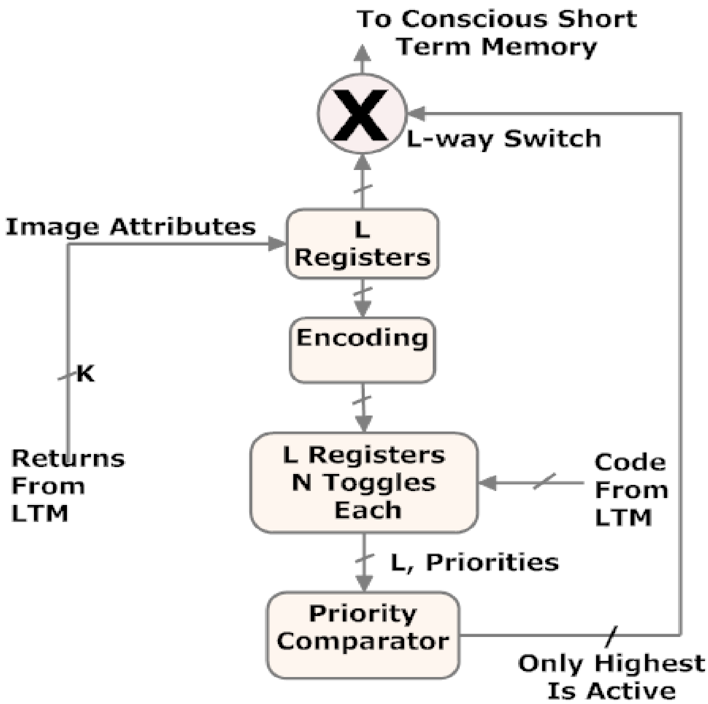

Figure 12: Return Editing Plan

OVERVIEW OF A MENTAL PROCESS

The major components of a system of physical consciousness are envisioned as in Figure 13. The cycle in the figure may be termed a cybernetic process, since returns from memory affect what is recalled next. The process works automatically, subconsciously, and perhaps several times per second to achieve consciousness.

Cues are taken from short-term memory, and are applied to find associated images stored in long-term memory. Memory search is subliminal and rapid, since essentially all stored images are queried in parallel.

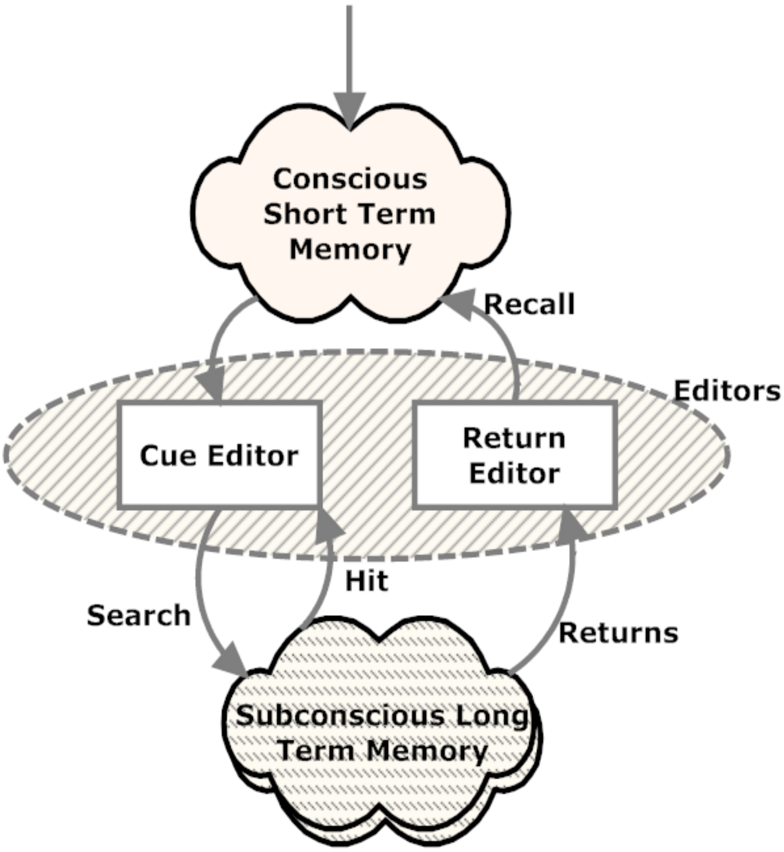

Figure 13: Overview of Brain System for Physical Consciousness

Normally it is expected that several images will be returned, especially because cues normally are inexact. Fortunately, a multi-match system is at work to help solve this problem. Images are returned in single file, to be held temporarily in registers of controlled toggle neurons. These registers have the ability to compute, for each image in parallel, a priority, using important attributes in each image. Only that image with the highest priority is permitted into consciousness.

Cues are derived from "conscious" short-term memory. A cue editor is important, since inconsistent cues are thought to be fairly common. Inconsistent cues result in mental blocks which could impair a person's ability to respond to danger. To help solve this problem, an uncomplicated system of cue editing is available. It involves removing a few cues randomly and repeating the memory search. If there continue to be no recalls, the removed cues are restored and another few cues are removed randomly, and the search repeats. A method by which neurons might accomplish the necessary editing and searching has been suggested above.

CONCLUSIONS

Circuit theory strongly suggests certain requirements on neurons that would not be disclosed by ordinary studies of molecular behavior. For instance, weak synapses to give single pulses are required, as covered above.

Single pulses also support a toggle-neurons, which may be triggered between rest (false) and active (true). Active means generating a stream of pulses, the result of an axon that connects via a weak synapse, and delay, back to one of its own dendrites. It is found via simulation (covered in the references) that a single neuron may easily develop into a toggle neuron.

Toggle neurons promise amazing mental operations, and are postulated to be essential to everyday editing operations within a conscious brain. Editing operations include cue editing to ensure a given memory is found within associative long-term memory, and return editing, when there are several returns, to ensure that a single important memory is forwarded into consciousness, as discussed above.

Experts and non experts alike have long desired a physical explanation of consciousness based on a physical interconnection of neurons, and such an explanation is attempted above. This paper grew from a great deal of past effort [1-50]. Neurons as above are chiefly asynchronous, and therefore not simple (like the synchronous systems within today's computers). Nevertheless, studies of complex, asynchronous physical systems are necessary to discover the exact nature of consciousness, and this may someday lead to tangible medical, psychological and scientific benefits.

Positive minded readers will see major opportunities for increased research and subsequent understanding in the above work. For instance, a deeper investigation of weak synapses is called for, since these are needed in a practical mental system. Also, further study of toggle neurons is in order, because of their immense computational potential. Furthermore, it should be worthwhile to look into the subconscious editing of cues and returns, as well as the relationship between short-term memory and consciousness. Much remains to be done, but eventually, neuroscience will benefit substantially from these budding efforts within the NCAS (Neural Circuits and Systems) field.

ATTACHMENT 1

Combinational Logic for Neurons

Neural logic within dendrites is termed *dendritic logic*. The simplest forms of dendritic logic are now described, although other forms exist.

Dendritic OR Gate

This is an uncomplicated physical junction of dendritic branches as in Figure 1A.

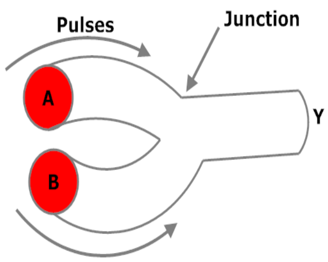

Figure 1A: Dendritic OR Gate

The Boolean expression is: ***Y = A+B***

Y, A, B are Boolean variables: ***False = 0, True = 1***. Note that under Boolean addition: ***1 + 1 = 1***. Consequently, the output ***Y*** computes as true if either or both of ***A, B*** are true. The OR gate is not dependent upon pulse coordination; pulses arriving at differing times are naturally passed through.

Dendritic AND Gate

Dendrites have their membranes exposed to surrounding salt solutions, and are generally active, but there could be a passive junction region in the above figure if the junction were insulated in some way. Propagation of a voltage pulse down the membrane from branch **A** to the trunk **Y** would be greatly slowed in a passive region. Some limited charge would trickle through, not enough to trigger the active membrane at output **Y**.

But if both branches **A** and **B** have simultaneous voltage pulse inputs, **A** and **B** work together, and there is enough voltage accumulation at **Y** to trigger pulses. The result is an AND gate, expressed as:

$$Y = A \bullet B$$

This is ordinary multiplication so if ***A*** and ***B*** are both true (1), the output ***Y*** computes to be true. But if either or both ***A, B*** is false (0), the output computes to be false. The dendritic AND gate is dependent upon pulses arriving at the junction at about the same time.

Dendritic XOR Gate

Computerized simulations indicate that the above OR may become an exclusive OR, meaning that any one signal will be transmitted, but that two applied together simultaneously will not be transmitted forward. This behavior depends of the fact that two colliding neural pulses arriving at the same time from ***A*** and ***B*** tend to cancel, or annihilate each other, meaning nothing is left to be transmitted. This is found to occur especially when the junction has a higher that average membrane capacitance. The Boolean equation for the exclusive OR, known as the XOR is:

$$Y = A \oplus B$$

The symbol $\oplus$ means:

$$Y = A\,B' + A'\,B$$

The prime ***A'*** means "invert"; that is, if ***A*** is true, it goes false, and if ***A*** is false, it goes true. The prime indicates a NOT operation. Note that the dendritic XOR requires that pulses arrive at about the same time.

It is interesting to note that if ***B*** is pre charged to true, then $B = 1$ and $B' = 0$; a NOT gate results:

$$Y = A'$$

The XOR will function as an inverter if one input be pre-activated to be true. It is significant that dendrites are very extensive, so thousands of dendritic gates are theoretically possible in a given neuron.

Enabled Logic

Enabled logic means that pulses slowly charge a larger capacitance until a triggering threshold is reached, usually the capacitance of a soma. Thus enabled logic, which depends on capacitive charge, differs from dendritic logic. For example, an enabled AND gate could have one input deliver part of the charge, and another input deliver another part of the charge, enough to trigger a pulse burst in the soma. Pulses need not arrive simultaneously, but must arrive before accumulated charge dissipates. Given only one soma per neuron, we expect far fewer enabled gates per neuron. Note for future reference that each positive neural pulse has a fixed amount of positive charge, approximately. Negative pulses are not possible in neurons.

Enabled NOT Gate

Without the availability of negative weighting factors as commonly assumed in artificial neurons, one wonders if a neural NOT gate is even possible. Figure 1B shows how it can be done. First the **b** input be pre-activated with a pulse burst. Then excitatory neurotransmitters are released at **a** and concurrently, inhibitory neurotransmitters at **c**. The inhibitory neurotransmitters from **c** will stop propagation down branch **b**. They also stop pulses from **a** (which is mentioned mainly for clarity).

If the pulses at **a** are removed, the inhibitory neurotransmitters from **c** are also removed, since **a** and **c** are linked. This permits the pulses applied to **b** to trigger the soma and produce an output, the result being a NOT gate:

$Z = a'$

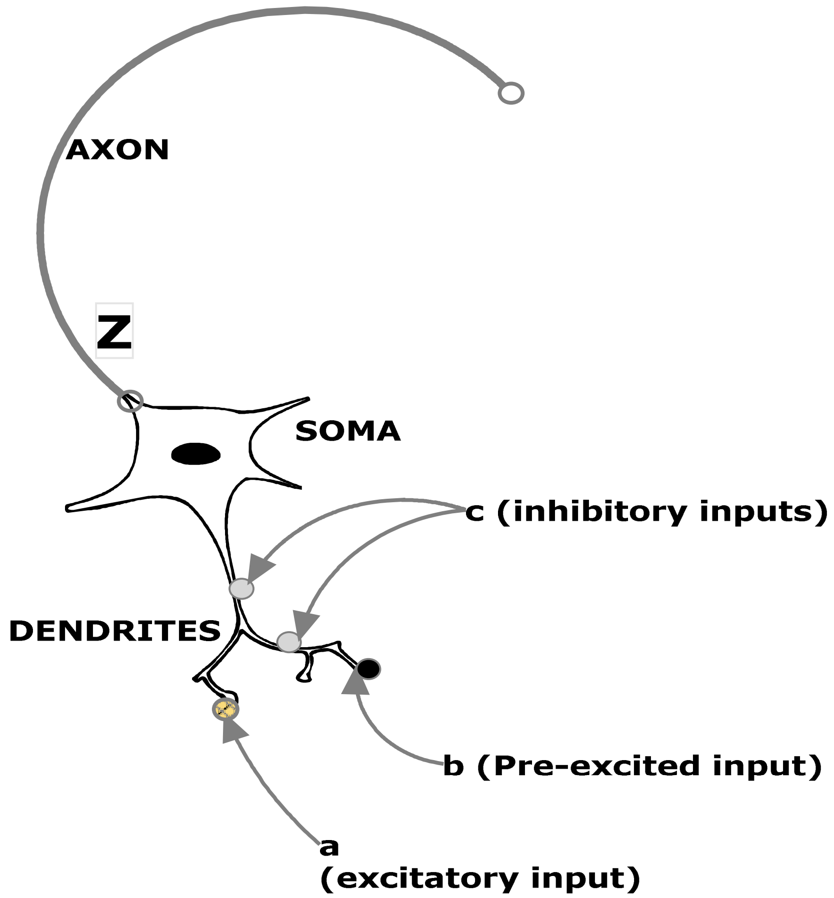

Figure 1B: Enabled NOT Gate

ATTACHMENT 2

A System for Long-term Memory

A standard memory element (Figure 2A) is one that will connect to other identical blocks to store images (or form "words"), where many such words constitute a large associative memory system. In an associative memory system, cues are applied up to ***K*** in number; these subsequently propagate throughout the entire memory system in a search for matches.

Cues are provided on a bundle of neural axons referred to below as the *x-bus*.

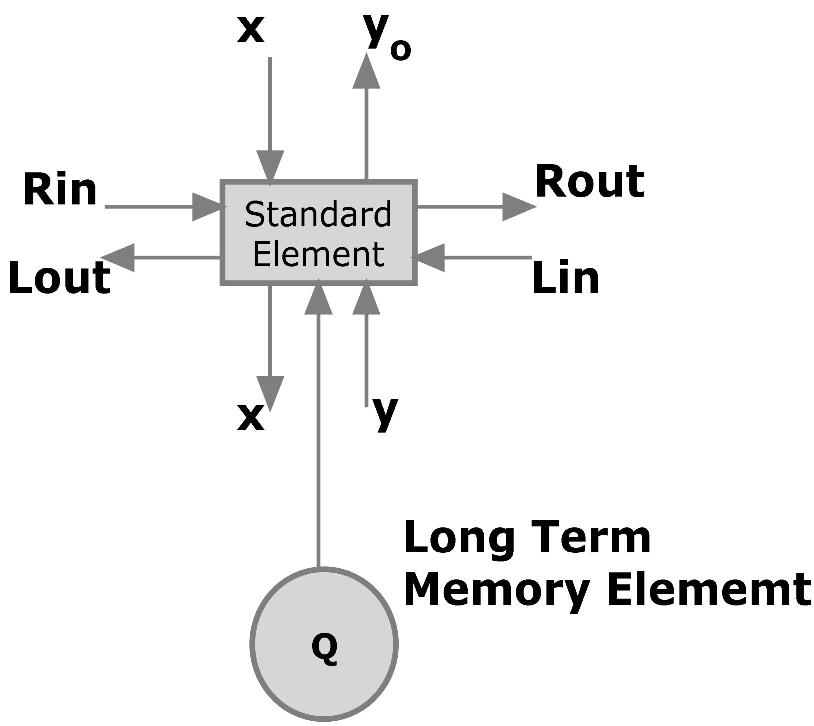

Figure 2A: Standard Memory Element

The approach below, not the only approach, is to develop a system with as few logical connections as possible. The plan is, the x-bus is going to be used to search for matches (to active cues only) in each word of long-term memory. All words are searched for active cues in parallel, approximately.

When a match occurs, it is going to be returned via the y-bus. Like the x-bus, the y-bus also holds K possible attributes transmitted on axons flowing up from long-term memory.

An outline of specifications follows: Returns are not permitted until the occurrence of an enable signal E. After E is applied, each word that contains a match to the true cues will produce memory done signals labeled Lout and Rout. A diagram (not a physical picture) of a memory word appears in Figure 2B.

Each block in the diagram has a long-term memory element, Qi , $1 \leq i \leq K$, that holds a true (or false) to define the attributes of a particular image. To query an image, an enable E is applied both on the left and right (Lin, Rin). Internal logic permits the E signals to ripple through the word in a search for matching attributes. Only when both left and right signals arrive at a given element of memory, and also only when conditions are satisfied relative to what is held by Qi will it have the potential to be connected to the y-bus. The end result is, there are no outputs to the y-bus unless there is a definite match to all of the true cues on the x-bus. A definite match to all of the active cues is indicated by the emergence from the word of Lout and Rout.

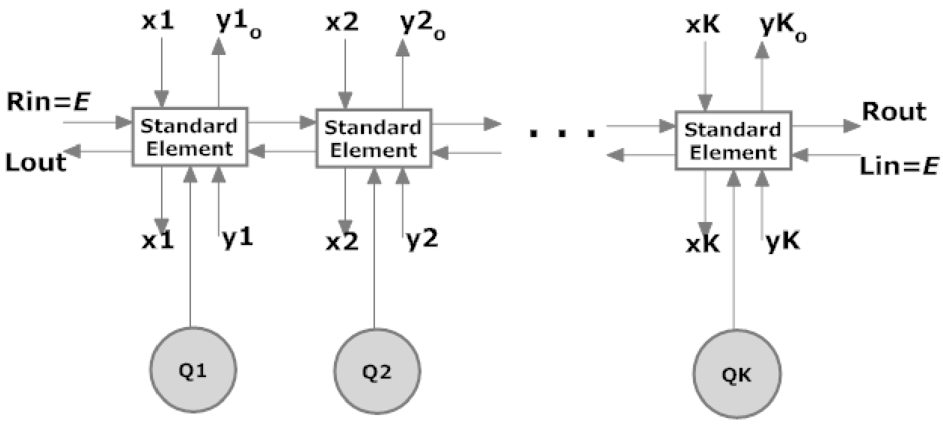

Figure 2B: Plan for Associative Memory

Note that the *x-bus* is forwarded "down" throughout the entire memory system, and the *y-bus* goes "up" throughout the entire memory system. Assuming only one match is found, the values in the *y-bus* coming from below can be assumed to be false (at rest). For more than one match, or return, the logic will force the y-bus signals coming from below to be false until it is their turn to be returned (refer to the system associated with Figure 8). When matches from below are returned, the words above are made transparent.

A standard memory element may be synthesized as follows. In Boolean algebraic terms, if there is no bus signal coming from the left ($Rin_i = 0$), then none must be transmitted to the right ($Rout_i = 0$). This keeps a memory word dormant until needed. If there is no cue, or if the cue is zero ($x_i = 0$), then within an individual element: $Rout_i = Rin_i$; in this case the memory Q_i may be either 0 or 1. If there is a cue for an attribute such that $x_i = 1$, but there is no memory of this feature in this word, or $Q_i = 0$, then bus signals must terminate ($Rout_i = 0$). If a cue for an attribute is active ($x_i = 1$) and also memory of this attribute is active ($Q_i = 1$) then $Rout_i = Rin_i$. Below is a Boolean equation for Rout, derived using standard logic symbols: **{•, +, ′}** for **{AND, OR, NOT}**

$$Rout_i = Rin_i \bullet [x_i' + Q_i]$$

A similar equation applies for $Lout_i$ in terms of Lin_i where $1 \le i \le K$.

Readout Logic

The output of a standard memory element is yio. This output will be true only if both Routi and Louti at the location of a given element are true, and also if Qi is active. The standard elements are organized in such a way that Routi and Louti cannot both be active unless there is a match within the word.

yio = yi + Routi ● Qi ● Louti

Normally yi is False (zero), or it is held false during multi match resolution. Figureure 2C summarizes the above requirements in circuit form (for an element labeled "i"). Note that either Rout or Lout from the end of the searched word may serve as a "***Hit"*** signal in a memory system, indicating to a cue editor, and a return editor, that there is a match to the active cues.

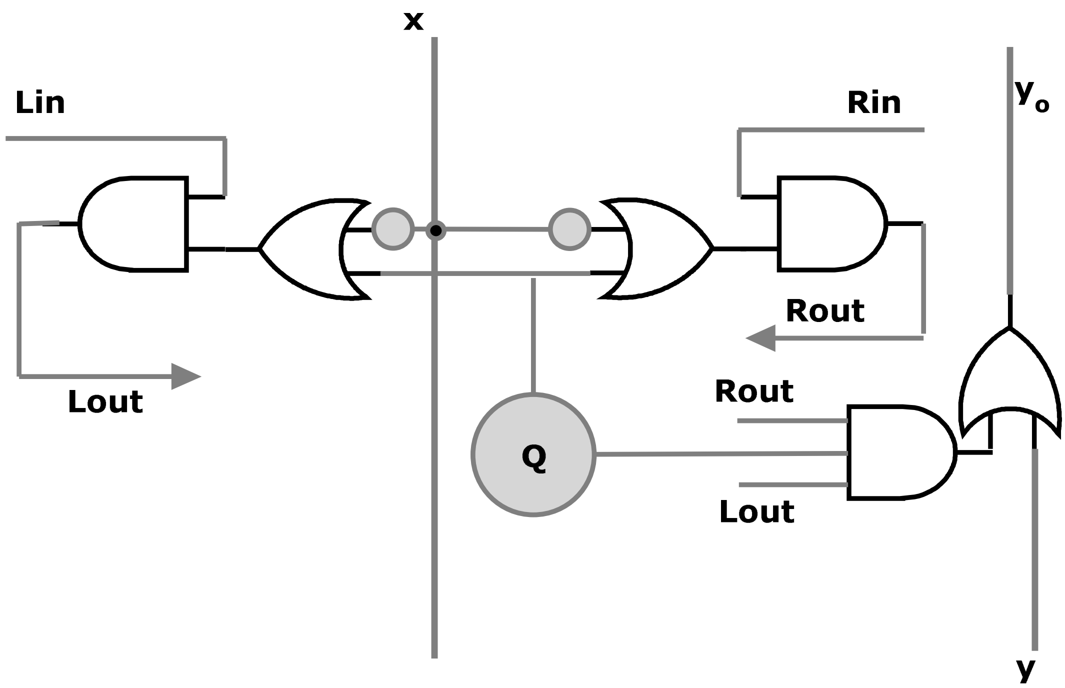

Figure 2C: Logic for a Standard Cell, Cell "i" of Long-term Memory

Note again that this simplified system works only with active cues. A large number of active cues are assumed to identify the sought after image with a high probability. Extraneous images, if any, are assumed to be tolerated, or possibly rejected by the return editor.

ATTACHMENT 3

Sequential Logic Using Neurons

A recursive neural circuit, as in Figure 3A, once started, generates a pulse train that can be interpreted to be logical **true**. A weak excitatory synapse, denoted by the triangle symbol, injects a single pulse back into the dendrite of the neuron. The pulse thus circulates until it is stopped, possibly by breaking the loop.

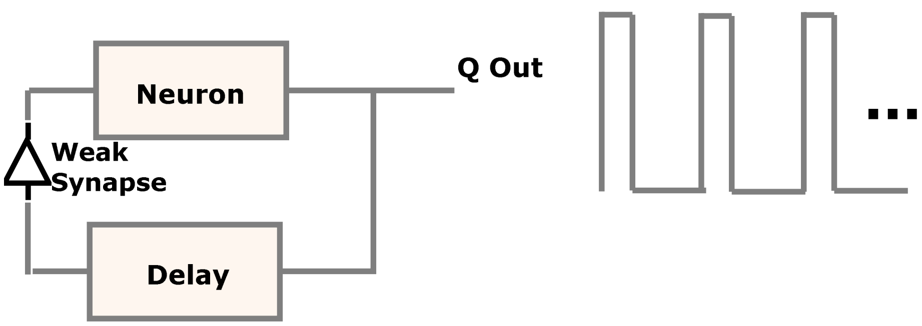

Figure 3A: Diagram of a Recursive Neuron

A recursive circuit as above may be made to toggle such that if it is **true,** it will be triggered to **False** (rest), and vice versa, if it is **False,** it will be triggered to **True** (active). Described below is one of the simplest possible toggling neurons, although certainly not the only possible toggling neuron.

Excitory/Inhibitory Toggling

The plan is to excite a circulating pulse at one point in a loop, and simultaneously to inhibit pulse propagation at a different (well chosen) point in the loop. Figure 3B illustrates the plan. Synapse S1 is a *weak excitatory synapse*, often modeled as injecting positive charge. The blocks labeled Delay1, 2, 3 and 4 represent the natural delays in a neural path.

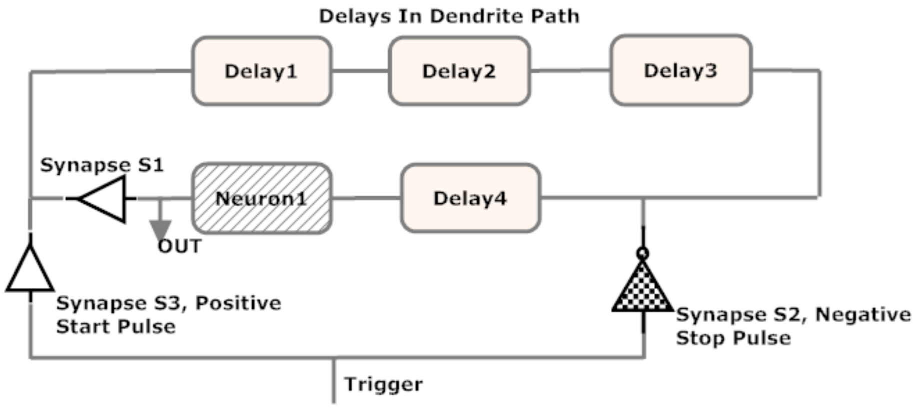

Figure 3B: Excitory-Inhibitory Toggling

Synapse S2 is a weak inhibitory synapse, often modeled as injecting negative charge; it serves to stop a circulating pulse. S3 is a weak excitatory synapse that serves to begin a circulating pulse. A trigger applied simultaneously to both synapses S2 and S3 will toggle this circuit. Simulations indicate that negative charge injection by S2 has little effect on a pulse initiated by S3, because the region near S2 is already charged negatively and for practical purposes is at rest when the circulating pulse arrives.

However, when a pulse is circulating, another trigger will stop the cycling. Circulation stops because charge is drained from a wide region surrounding S2, taking necessary charge away from the circulating pulse. This terminates the pulse propagation.

Controlled Toggling

A *controlled toggle* is one that toggles if and only if one or more control signals are true. A controlled toggle is simple enough to achieve with a neural AND as in Figure 3C. The output at the top serves to trigger a toggling neuron.

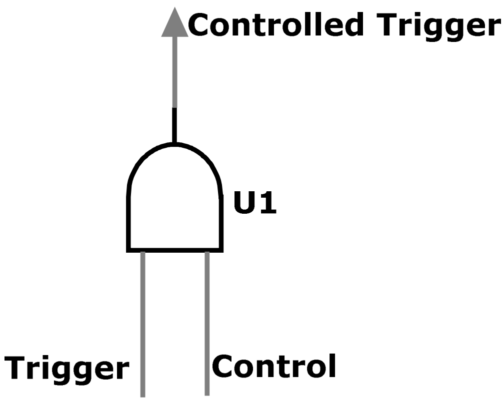

Figure 3C: Controlled Trigger

Controlled toggles amount to long-term memory with computational possibilities, and are important to mental processing.

In a computational system, additional neural gates are utilized. Figure 3D suggests that a "source" signal enables the output of a given toggle to be applied to a bus composed of interneurons. Then a "target" signal selects one or more other elements that need to be toggled in response to the particular source signal, to accomplish a given calculation.

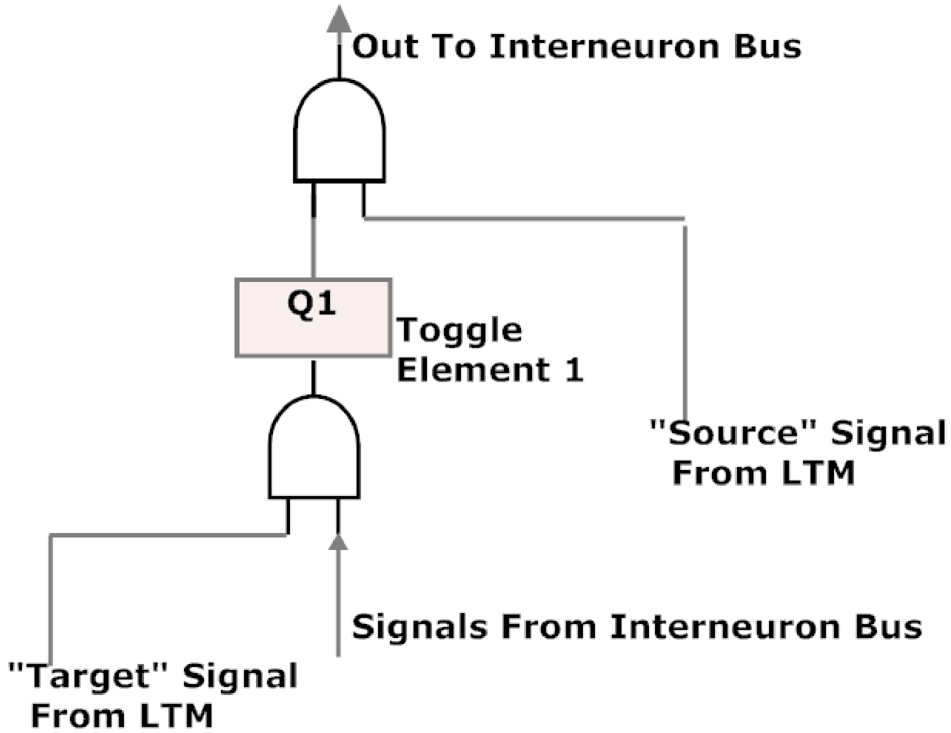

Figure 3D: Controlled Toggle Element in a Neural System

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APPENDICES

About John Robert Burger

Dr. Burger

John Robert Burger (1940 -)

John Robert Burger was the first of seven children born on a farm in Marion, in Western New York to Margaret Mary Schaefer and Robert James Burger. After high school, he worked as a draftsman, saved his money and was able to attend the State Technical Institute at Alfred, New York. Upon finishing a two-year degree, he accepted a position far from home in Albuquerque New Mexico, as a Health Physics technician for Sandia Corporation.

Sandia Corporation allowed Burger to collect sufficient funds to transfer to Clarkson College of Technology in Potsdam, New York where he earned a Bachelor of Science degree in Electrical Engineering in 1964. With the help of a Sloan Foundation Grant, he earned the Master of Science degree in Nuclear Engineering in 1967 from the University of California at Berkeley. While at UCLA he was supported in part by a TRW Doctoral Fellowship, gaining a Doctor of Philosophy in Electrical and Computer Engineering in 1978 specializing in circuits and systems.

Burger became an Assistant Professor in Electrical Engineering at the University of the Pacific in Stockton, California in 1979. He achieved the position of Professor in 1988 in the Department of Electrical and Computer Engineering, California State University, Northridge, California thanks to help from Dr. Raymond Pettit, department Chair.

Burger was a teaching Professor at CSUN for most of his professional life including a visit to the Oregon Institute of Technology at Klamath Falls, between 1999 and 2001 to develop their computer systems engineering technology degree. Over the years Dr. Burger and his students have pursued integrated circuit and computer design, with the help of grants from MOSIS (Metal Oxide Semiconductor Implementation Service).

In addition to his research, he enjoys amateur radio (WB6VMI), playing traditional music on the fiddle and Scottish country dancing. Burger is the father of two children: Terry John born in 1977 and Heather Mary born in 1981; he currently resides in Eugene, Oregon.